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09/651,159	08/30/2000	Ole Bentz	MTI-31072	2115

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EXAMINER	
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ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,159	BENTZ, OLE	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005 and 08 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5 and 10-12* is/are allowed.

6)☒ Claim(s) *1-3, 6-9, 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

TODD INGBERG
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/08/2005.

2. Claims 1-20 are pending in this application. Claims 1-4, 6-7, and 9-16 are independent claims. This Office Action is made non-final after a RCE filed 10/19/2005.

Drawings

3. The drawings are objected to because the specification does not disclose an inverter in Figure 2 for inverting a MSB result prior entering an OR. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 9, it is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "the most significant bit of the result is logically inverted prior to the logically ORing" in lines 12-13 was not described any in the specification in order to produce a correct result of an overflow selection flag. For examination purposes, the examiner disregards this limitation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-9, 13-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being obvious over Bonnet et al. (U.S. 6,321,248) in view Jain et al. (U.S. 6,061,781).

Re claim 1, Bonnet et al. disclose in Figure 1 a method of detecting overflow in a clamping circuit (e.g. abstract), comprising: inputting a first operand having a first fixed-point format into the clamping circuit (e.g. A as first operand in circuit in Figure 1 and col. 3 lines 37-68 as fixed-point format wherein A_L as fractional bits; and col. 3 lines 23-31); inputting a second operand having a second fixed-point format into the clamping circuit (e.g. B as second operand in circuit in Figure 1 and col. 3 lines 37-68 as fixed-point format wherein B_L as fractional bits; and col. 3 lines 23-31); determining (e.g. circuit 4 in Figure 1) an overflow output based upon the first and second fixed-point format (e.g. A_H and B_H are input into 4 in Figure 1) and predicting whether an arithmetic operation of the first operand with the second operand will yield a result that exceeds the overflow output (e.g. col. 3 lines 2-22 and col. 1 line 40 to col. 2 line 12); performing at least partially the arithmetic operation of the first and second operands (e.g. E1 in Figure 1); inputting the result and overflow output into a multiplexor for selection there between (e.g. inputs into 4 in Figure 1 wherein the S as result and VALSAT* and VALSAT as overflow outputs); wherein the determining an predicting occurs independent from and

substantially in parallel with the performing (e.g. col. 1 lines 47-54). Bonnet et al. fail to disclose the step of discontinuing the performing if the result exceeds the overflow output. However, Jain et al. disclose the step of discontinuing the performing if the result exceeds the overflow output (e.g. col. 16 lines 47-65, particularly lines 57-61). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a step of discontinuing the performing if the result exceeds the overflow output as seen as a concept in Jain et al.'s invention into Bonnet et al.'s invention because it would enable to minimize the power and cost attributes in circuit (e.g. col. 16 lines 47-65).

Re claim 2, it has same limitations as cited in claim 1. Thus, claim 2 is rejected under the same rational as cited in the rejection of claim 1. In addition, Bonnet et al. further disclose in Figure 1 the arithmetic operation as a multiplication operation (e.g. col. 5 lines 40-45).

Re claim 3, it has same limitations as cited in claim 2. Thus, claim 3 is rejected under the same rational as cited in the rejection of claim 2. In addition, Bonnet et al. further disclose in Figure 1 a step of substituting (e.g. through a multiplexer 2 in Figure 1) the operation result (e.g. S) with the clamping value (e.g. either VALSAT* or VALSAT) when it is determined that the operation result will exceed the representable value (e.g. col. 10 lines 25-39).

Re claim 6, Bonnet et al. disclose in Figure 1 a method of processing multiplier data paths (e.g. abstract and col. 5 lines 40-45), comprising: performing at least a partial multiplication of a plurality of operands (e.g. col. 5 lines 40-45), each having a fixed-

point format (e.g. A and B as first and second operand in circuit in Figure 1 and col. 3 lines 37-68 as fixed-point format wherein A_L and B_L as fractional bits; and col. 3 lines 23-31); determining whether the at least partial multiplication of the operands produces a product that will exceed a pre-determined limit based upon the fixed-point format of each of the operands (e.g. col. 10 lines 25-38 which carry out by the circuit 4 in Figure 1); wherein the determining an predicting occurs independent from and substantially in parallel with the performing (e.g. col. 1 lines 47-54). Bonnet et al. fail to disclose the step of discontinuing the performing if the result exceeds the overflow output. However, Jain et al. disclose the step of discontinuing the performing if the result exceeds the overflow output (e.g. col. 16 lines 47-65, particularly lines 57-61). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a step of discontinuing the performing if the result exceeds the overflow output as seen as a concept in Jain et al.'s invention into Bonnet et al.'s invention because it would enable to minimize the power and cost attributes in circuit (e.g. col. 16 lines 47-65).

Re claim 7, Bonnet et al. disclose in Figure 1 a method of clamp detection (e.g. abstract), comprising: inputting a first and a second operands (e.g. A and B in Figure 1) to both a multiplier (e.g. 1 in Figure 1 wherein the arithmetic unit is a multiplier as cited in col. 5 lines 40-45) and an overflow detection circuit (e.g. 4 in Figure 1); multiplying the first and second operands to generate a result not to exceed a predetermined number of bits (e.g. col. 3 to col. 4); determining an initial clamping predictor bit based upon the first operand and the second operand (e.g. operation of 4 in Figure 1 and col. 6 to col.

10); and logically ORing (e.g. col. 2 lines 1-12) the initial clamping predictor bit (e.g. A_H + B_H in col. 2 lines 1-12) and a most significant bit of the result (e.g. $Cout_{n-2}$) to produce a final clamping predictor bit (e.g. output of 4 with either Non-sat, sat, or sat* in Figure 1); inputting the result into a multiplexor (e.g. 2 in Figure 1); and wherein the multiplying and determining steps occur independently and substantially in parallel (e.g. col. 1 lines 47-54). Bonnet et al. fail to disclose the step of discontinuing the performing if the result exceeds the overflow output. However, Jain et al. disclose the step of discontinuing the performing if the result exceeds the overflow output (e.g. col. 16 lines 47-65, particularly lines 57-61). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a step of discontinuing the performing if the result exceeds the overflow output as seen as a concept in Jain et al.'s invention into Bonnet et al.'s invention because it would enable to minimize the power and cost attributes in circuit (e.g. col. 16 lines 47-65).

Re claim 8, Bonnet et al. further disclose in Figure 1 the first and second operands are in a fixed-point format (e.g. A and B as first and second operand in circuit in Figure 1 and col. 3 lines 37-68 as fixed-point format wherein A_L and B_L as fractional bits; and col. 3 lines 23-31).

Re claim 9, it has same limitations cited in claim 7. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of claim 7.

Re claim 13, Bonnet et al. disclose in Figure 1 a multiplication overflow detection circuit (e.g. abstract) comprising: multiplication circuitry for at least partially multiplying a first and a second operand (e.g. 1 in Figure 1 wherein the arithmetic unit is a multiplier

as cited in col. 5 lines 40-45); and overflow detection circuitry (e.g. 4 in Figure 1) receiving the first and second operands (e.g. A and B respectively) that detects whether a result of the multiplication of the first and second operands exceed a maximum representable positive or negative value (e.g. col. 10 lines 25-39); wherein the multiplication circuitry and the overflow detection circuitry operate independently and substantially in parallel (e.g. col. 1 lines 47-54); the result is input into a multiplexor (e.g. 2 in Figure 1). Bonnet et al. fail to disclose the step of discontinuing the performing if the result exceeds the overflow output. However, Jain et al. disclose the step of discontinuing the performing if the result exceeds the overflow output (e.g. col. 16 lines 47-65, particularly lines 57-61). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a step of discontinuing the performing if the result exceeds the overflow output as seen as a concept in Jain et al.'s invention into Bonnet et al.'s invention because it would enable to minimize the power and cost attributes in circuit (e.g. col. 16 lines 47-65).

Re claim 14, Bonnet et al. further disclose in Figure 1 the overflow detection circuitry utilizes a fixed-point format of the first and second operands to determine whether the result of the multiplication exceeds the maximum representable positive or negative value (e.g. col. 6 to col. 10).

Re claim 15, it is a circuit claim of claim 7. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of claim 7.

Re claim 16, it has same limitations cited in claim 15. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of claim 15. In addition,

Bonnet et al. further disclose in Figure 1 a multiplexer (e.g. 2 in Figure 1 and col. 10 lines 25-40) comprising: a clamp value input for receiving a clamp value to be output when clamping occurs; a clamp bit register input connected to the clamp bit register for receiving the clamp bit (e.g. VALSAT* and VALSAT); a result register input connected to the result register for receiving the result of the multiplication of the first and second operands (e.g. output of 1 in Figure 1); and an output (e.g. output of 2 in Figure 1); the multiplexer select one of the clamp value register input and the result register input based upon a logical level of the clamp bit register in order to make the selected input the output of the multiplexer (e.g. 4 in Figure 1 and col. 10 lines 25-40).

Re claim 17, it has same limitations cited in claim 15. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of claim 15. In addition, Bonnet et al. further disclose in Figure 1 the clamp bit input is logically ORed with a most significant bit of the result stored in the result register (e.g. col. 2 lines 1-12).

Re claim 19, it is a circuit claim of limitations cited in claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of claim 8.

Re claim 20, Bonnet et al. further disclose in Figure 1 determing whether clamping occurs based upon a logical value of the final clamping predictor bit and selecting one of a pre-selected clamp value and the result of the multiplying (e.g. 4 and 2 in Figure 1 and col. 10 lines 25-40)

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Bonnet et al. (U.S. 6,321,248) in view Jain et al. (U.S. 6,061,781), as applied to claim 15, in further view of Kim (U.S. 5,369,438).

Re claim 18, Bonnet et al. in view of Jain et al. fail to disclose the register as a flip-flop. However, Kim discloses the flip-flop as register for latching input data (e.g. col. 4 lines 41-50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the register as a flip-flop as seen in Kim's invention into Bonnet et al. in view of Jain et al.'s invention because it would enable to simplify the circuitry.

Allowable Subject Matter

9. Claims 4-5 and 10-12 are allowed.

Response to Arguments

10. Applicant's arguments with respect to claims 1-3, 6-8, and 13-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 23, 2006

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